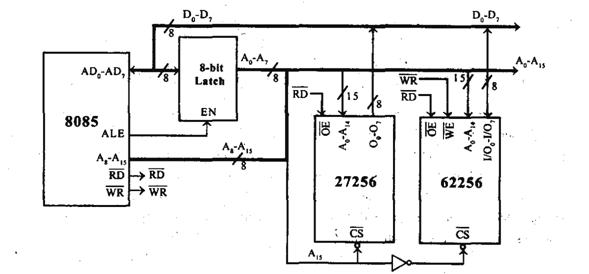
**EXAMPLES OF MEMORY INTERFACING (Contd..)**

**EXAMPLE-2**

**Consider a system in which the available 64kb memory space is equally divided between EPROM and RAM. Interface the EPROM and RAM with 8085 processor.**

* **Implement 32kb memory capacity of EPROM using single IC 27256.**
* **32kb RAM capacity is implemented using single IC 62256.**
* **The 32kb memory requires 15 address lines and so the address lines A0 - A14 of the processor are connected to 15 address pins of both EPROM and RAM.**
* **The unused address line A15 is used as to chip select. If A15  is 1, it select RAM and If  A15  is 0, it select EPROM.**
* **Inverter is used for selecting the memory.**
* **The memory used is both Ram and EPROM, so the low RD and WR pins of processor are connected to low WE and OE pins of memory respectively.**
* **The address range of EPROM will be 0000H to 7FFFH and that of RAM will be 7FFFH to FFFFH.**

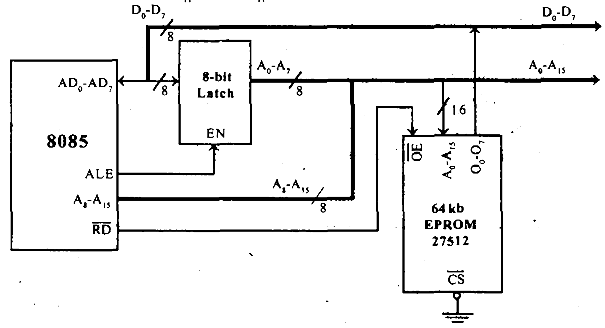


**Fig.- Interfacing 32Kb EPROM and 32Kb RAM with 8085**

**EXAMPLE-1**

**Consider a system in which the full memory space 64kb is utilized for EPROM memory. Interface the EPROM with 8085 processor.**

* **The memory capacity is 64 Kbytes. i.e**
* **2^n = 64 x 1000 bytes where n = address lines.**
* **So, n = 16.**
* **In this system the entire 16 address lines of the processor are connected to address input pins of memory IC in order to address the internal locations of memory.**
* **The chip select (CS) pin of EPROM is permanently tied to logic low (i.e., tied to ground).**
* **Since the processor is connected to EPROM, the active low RD pin is connected to active low output enable pin of EPROM.**
* **The range of address for EPROM is 0000H to FFFFH.**

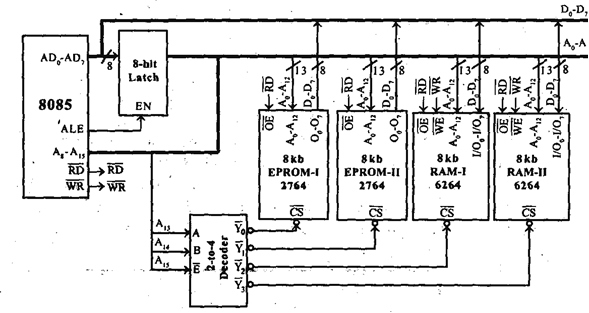


**Fig.:Interfacing 64Kb EPROM with 8085**

**EXAMPLE-3**

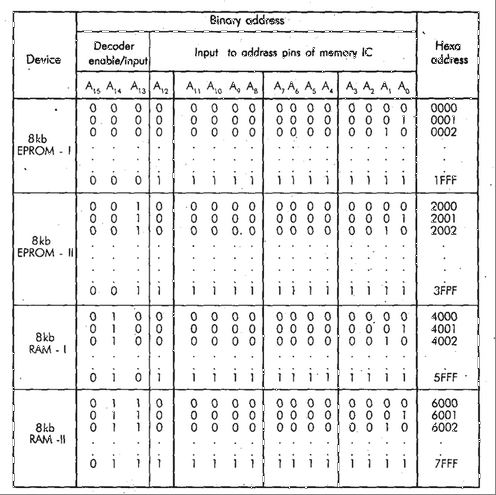
**Consider a system in which 32kb memory space is implemented using four numbers of 8kb memory. Interface the EPROM and RAM with 8085 processor.**

* **The total memory capacity is 32Kb. So, let two number of 8kb n memory be EPROM and the remaining two numbers be RAM.**
* **Each 8kb memory requires 13 address lines and so the address lines A0- A12 of the processor are connected to 13 address pins of all the memory.**
* **The address lines and A13 - A14 can be decoded using a 2-to-4 decoder to generate four chip select signals.**
* **These four chip select signals can be used to select one of the four memory IC at any one time.**
* **The address line A15 is used as enable for decoder.**
* **The simplified schematic memory organization is shown.**



**Fig: Interfacing 16Kb EPROM and 16Kb RAM with 8085**

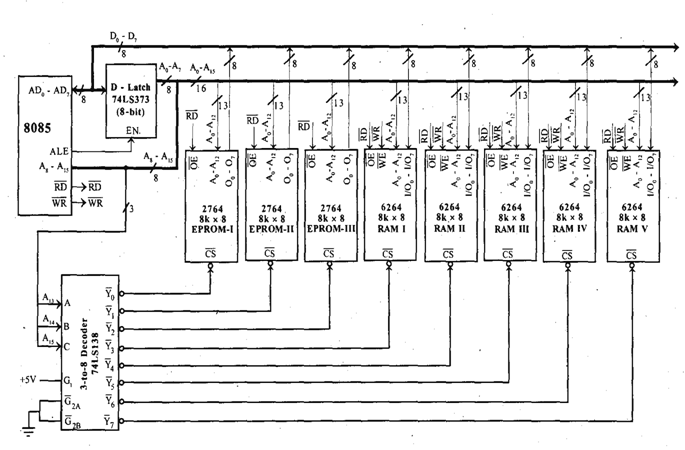
**The address allotted to each memory IC is shown in following table.**



**EXAMPLE-4**

**Consider a system in which the 64kb memory space is implemented using eight numbers of 8kb memory. Interface the EPROM and RAM with 8085 processor.**

* **The total memory capacity is 64Kb. So, let 4 numbers of 8Kb EPROM and 4 numbers of 8Kb RAM.**
* **Each 8kb memory requires 13 address lines. So the address line A0 - A12 of the processor are connected to 13address pins of all the memory lCs.**
* **The address lines A13, A14 and A]5 are decoded using a 3-to-8 coder to generate eight chip select signals. These eight chip select signals can be used to select one of the eight memories at any one time.**
* **The memory interfacing is shown in following figure.**



**Fig- Interfacing 4 no. 8Kb EPROM and 4 no. 8Kb RAM with 8085**

**The address allocation for Interfacing 4 no. 8Kb EPROM and 4 no. 8Kb RAM with 8085 is,**

